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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,525	03/08/2002	Keishiro Okamoto	020214	3829

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,525	OKAMOTO ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation of "a wiring layer formed on or above said support substrate, leading some of said through holes filled with conductor upwards via said capacitor, having branches" is not clear as to what it means. It is not clear how the wiring layer leads some of the through holes filled with conductors upwards via the capacitor without shorting the capacitor. Furthermore it is not clear whether the branches belong to the capacitor or the wiring layer.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-6, 8-10 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al., US patent No. 6,503,778 in view of Gnadinger, US patent No. 5,229,647.

Regarding claim 1, As best the examiner is able to ascertain the claimed invention, Yamauchi teaches (figs. 1, and 3A-27B) a semiconductor apparatus, comprising: a support substrate (39, 11, figs. 4A-4D, 9A and 9B) having through holes filled with conductor (19a, 19b and 19c) in conformity with a first uniform pitch, capacitors (20 and 40, col. 18, lines 53-61) formed on the support substrate (39), a wiring layer (the integrated circuit containing 20 inherently has wiring layer) formed on the support, leading some of the through holes filled with conductor upwards via the capacitor (20), having branches, the wiring layer having wires (dashed structures above 19a, 19b and 19c, refer to figs. 9A and 9B) of a second uniform pitch narrower than the first uniform pitch and plural semiconductor elements (wiring structures connected to the dashed structures) disposed on the wiring layer, having terminals in conformity with the second uniform pitch, and connected with the wiring layer via the terminals (figs. 9A and 9B).

Yamauchi does not teach a support substrate made of a semiconductor substrate.

Gnadinger teaches (fig. 4, col. 3, lines 37-57) the use of a semiconductor wafer (10) as a support in the structure of forming an interconnect structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the semiconductor substrate taught by Gnadinger in the structure of Yamauchi in order to form a high density interconnection structure.

Regarding claims 4 and 5, Yamauchi teaches (fig. 4A) substantially the entire claimed structure of claim 1 above including the support substrate is a Si substrate (10)

having through holes (refer to fig. 4 of Gnadinger) with an insulation film (24) formed on the side walls of the holes, and the through holes filled with conductor are metallic conductors packed in the through holes.

Regarding claim 6, Yamauchi teaches substantially (figs. 4 of Gnadinger, col. 3, lines 37-57) the entire claimed structure of claim 1 above including the insulation film is a silicon oxide film (24) and lower surfaces of the silicon substrate are also covered with an insulating material (27).

The limitation that the silicon oxide film is formed by thermal oxidation is not given patentable weight because, this is considered a product-by-process claim. "[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claims 8 and 9, Yamauchi teaches substantially the entire claimed structure of claim 1 above including the through holes filled with conductor (19A-19C) include a first signal wire the wiring layer contains a second signal wire (dashed structures) for leading the first signal wire substantially vertically; and the capacitor has electrodes (inherent characteristics of a capacitor) with a vacancy (region between the dashed structures) around a region where the second signal wire is located.

Regarding claim 10, Yamauchi teaches (figs. 4a-4d) substantially the entire claimed structure of claim 1 above except explicitly stating that the insulation layer disposed on the support substrate, have a thermal expansion coefficient of 10 ppm/°C or less in the in-plane direction, and insulates the wiring layer and the capacitor.

Parameters such as coefficient of thermal expansion and heat capacity in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thermal expansion coefficient of Yamauchi structure as claimed in order to improve the thermal property of the device.

Regarding claim 13, Yamauchi teaches (figs. 9A and 9B) substantially the entire claimed structure of claim 1 above including the wiring layer contains a wiring connecting the plural semiconductor elements with each other.

Regarding claim 14, Yamauchi teaches (figs. 4a-4d) substantially the entire claimed structure of claim 1 above including another circuit part (transistors between the wirings) connected with the wiring layer.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi, Gnadinger and in view of Malladi, US patent No. 5,939,782.

Regarding claim 2, Yamauchi teaches substantially the entire claimed structure of claim 1 above except explicitly stating a circuit board having wiring of a first uniform pitch and connected to lower surfaces of the through holes fills with conductor.

It is conventional and also taught by Malladi attaching a circuit board (50) (fig. 3) with a uniform pitch and connected to lower surfaces of through holes (64) with conductor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the circuit board connection taught by Malladi in the structure of Yamauchi in order to provide an IC package which provides a more convenient electrical interface with the outside world.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi, Gnadinger and in view of Kabumoto et al., US patent No. 5,883,428.

Regarding claim 7, Yamauchi teaches (fig. 1) substantially the entire claimed structure of claim 1 above except explicitly teaching that the capacitor is a decoupling capacitor connected between power wires.

Decoupling capacitors are conventional in the art and are also taught by Kabumoto (fig. 1) for reducing power-supply noise (col. 5, lines 23-48).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the decoupling capacitors taught by Kabumoto in the structure of Yamauchi in order to reduce noise between the power wires of Yamauchi's integrated device.

7. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi, Gnadinger and in view of Cuchiaro et al. US patent No. 5,888,585.

Regarding claims 11 and 12, Yamauchi teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the capacitor has a capacitor

dielectric layer made of an oxide containing at least one of Ba, Sr and Ti, and a pair of capacitor electrodes sandwiching the capacitor dielectric layer and containing at least partially one of Pt, Ir, Ru, Pd or any of their oxides.

Cuchiaro teaches a charge storage device including high dielectric material comprising barium and platinum electrode in the process of making an integrated device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitor structure of Yamauchi device using the materials taught by Cuchiaro in order to form a capacitor structure that is smaller in size and less leakage current.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 2 and 4-14 have been considered but are not persuasive. Applicant argues that Yamauchi does not aim to connect semiconductor elements of narrow terminal pitch with a circuit board of wide wiring pitch. As shown above in the rejection, Yamauchi teaches through holes filled with conductor (19a, 19b and 19c) in conformity with a first uniform pitch, and uses capacitor structures (20 and 40, col. 18, lines 53-61) formed on the support substrate (39), to connect with wiring layer (the integrated circuit containing 20 inherently has wiring layer) the wiring layer having wires (dashed structures above 19a, 19b and 19c, refer to figs. 9A and 9B) of a second uniform pitch narrower than the first uniform pitch and plural semiconductor elements (wiring structures connected to the dashed structures) disposed on the wiring layer, having terminals in conformity with the second

uniform pitch, and connected with the wiring layer via the terminals (figs. 9A and 9B). Therefore Yamauchi essentially teaches semiconductor elements having terminals of narrow pitch connected to a capacitor structure through wires of wide first pitch as shown above.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is (571)-272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-17321732. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
May 16, 2005

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800